Amendments to the Claims:

Please cancel claims 2, 3, 5-8, 10, 13, 17, 26-39, 41, 42, 44, 46, and 49. Please add new claims 51-55. Please amend claims 1, 4, 9, 11, 12, 14-16, 18-21, 23-25, 40, 43, 45, 47, 48, and 50 as follows.

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An image processing system, comprising:

an input for receiving an input signal; [[and]]

a correlated double sampler (CDS) for receiving the input signal, sampling the input signal, amplifying the input signal with a first gain, and providing an output signal, the CDS comprising an amplifier for amplifying the input signal with the first gain, the first gain being settable to one of a plurality of first levels based on a digital input signal; ~~and a variable capacitance unit having first and second variable input capacitances, the first variable input capacitance being connected to a first input of the amplifier and the second variable input capacitance being connected to a second input of the amplifier~~; and

a programmable gain amplifier (PGA) for receiving the output signal from the CDS and amplifying the received output signal, the PGA comprising a second amplifier for amplifying the received output signal with a second gain, the second gain being settable to one of a plurality of second levels based on the digital input signal, each of the first levels being divided into the second levels, and an overall gain of the system being determined by a combination of the first gain of the CDS and the second gain of the PGA.

2. – 3. (Cancelled)

4. (Currently Amended) The image processing system of claim 1, wherein the first gain in the CDS is settable to a level between 1.0 and 2.0.

5.-8. (Cancelled)

9. (Currently Amended) The image processing system of claim [[7]]1, wherein the second gain in the PGA is settable to a level between 1.0 and 2.0.

10. (Cancelled)

11. (Currently Amended) The image processing system of claim [[10]]1, wherein the digital input signal contains a plurality of bits.

12. (Currently Amended) The image processing system of claim 11, wherein ~~a first portion of the bits is applied to the CES to set the gain of the CDS and a second portion of the bits is applied to the PGA to set the gain in the PGA~~ the first gain of the CDS is settable to one of the first levels based on a first portion of the bits and the second gain of the PGA is settable one of the second levels based on a second portion of the bits.

13. (Cancelled)

14. (Currently Amended) The image processing system of claim [[13]]1, wherein the overall gain is pseudo-logarithmic.

15. (Currently Amended) An image processing system, comprising:

a correlated double sampler (CDS) for receiving an input signal, sampling the input signal, amplifying the input signal with a first gain, and providing ~~an~~ a first output signal, ~~the CDS comprising: an amplifier for amplifing the input signal and a variable capacitance unit having first and second variable input capacitances, the first variable input capacitance being connected to a first input of the amplifier and the second variable input capacitance being connected to a second input of the amplifier~~ the first gain being settable to one of a plurality of first levels based on a digital input signal; and

a programmable gain amplifier (PGA) for receiving the first output signal from the CDS and amplifying the first output signal with a second gain, and providing a second output signal, the second gain being settable to one of a plurality of second levels

based on the digital input signal, each of the first levels being divided into the second levels, and an overall gain of the system being determined by a combination of the first gain of the CDS and the second gain of the PGA.

16. (Currently Amended) The image processing system of claim 15, wherein ~~gain in the CDS is settable to one of a plurality of levels~~ the CDS comprises:

a first amplifier for amplifing the input signal;

a first capacitor unit having a first variable capacitance, and coupled to a first input of the first amplifier; and

a second capacitor unit having a second variable capacitance, and coupled to a second input of the second amplifier.

17. (Cancelled)

18. (Currently Amended) The image processing system of claim [[15]]16, wherein the first gain in the CDS is settable to a level between 1.0 and 2.0.

19. (Currently Amended) The image processing system of claim [[15]]18, wherein the PGA ~~in the PGA is settable to one of a plurality of levels~~ comprises:

a second amplifier for amplifying the first output signal:

a first plurality of switched capacitors having a third variable capacitance, and coupled to a first output terminal of the first amplifier and a first input terminal of the second amplifier; and

a second plurality of switched capacitors having a fourth variable capacitance, and coupled to second output terminal of the first amplifier and a second input terminal of the second amplifier.

20. (Currently Amended) The image processing system of claim [[15]]19, wherein the second gain in the PGA is settable to a level between 1.0 and 2.0.

21. (Currently Amended) The image processing system of claim [[15]]20, wherein ~~a gain in the CDS and a gain in the PGA are settable by a digital input signal~~ the first gain

is settable to one of the first levels by adjusting the first variable capacitance and the second variable capacitance based on the digital input signal, and the second gain is settable to one of the second levels by adjusting the third variable capacitance and the fourth variable capacitance based on the digital input signal.

22. (Original) The image processing system of claim 21, wherein the digital input signal contains a plurality of bits.

23. (Currently Amended) The image processing system of claim 22, wherein ~~a first portion of the bits is applied to the CDS to set gain in the CDS and a second portion of the bits is applied to the PGA to set gain in the PGA~~ the first gain in the CDS is settable to one of the first levels based on a first portion of the bits and the second gain in the PGA is settable to one of the second levels based on the second portion of the bits.

24. (Currently Amended) The image processing system of claim 15, wherein ~~an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA~~ the CDS comprises:

the first amplifier having an inverted input terminal, a non-inverted input terminal, an inverted output terminal, and a non-inverted output terminal;

a first capacitor unit coupled between the inverted input terminal and a first node, a first capacitance of the first capacitor unit varying in response to a first portion of a plurality of bits of the digital input signal

a first sampling switch for sampling a reference level signal of the input signal in response to a first sampling clock to output a sampled reference level signal to the first node;

a second sampling switch for sampling an image signal of the input signal in response to a second sampling clock to output a sampled image signal to the first node;

a second capacitor unit coupled between the inverted input terminal and the non-inverted output terminal, a second capacitance of the second capacitor unit having a unit capacitance value;

a third sampling switch serially coupled to the second capacitor unit to be turned on in response to the second sampling clock;

a third capacitor unit coupled between the non-inverted input terminal and a second node, a third capacitance of the capacitor unit varying in response to the first portion of a plurality of bits of the digital input signal;

a fourth sampling switch for sampling a first reference level signal in response to the first sampling clock to output a sampled first reference level signal to the second node;

a fifth sampling switch for sampling a feedback signal in response to the second sampling clock to output a sampled feedback signal to the second node;

a fourth capacitor unit coupled between the non-inverted input terminal and the inverted output terminal, a fourth capacitance of the second capacitor unit having the unit capacitance value; and

a sixth sampling switch serially coupled to the fourth capacitor unit to be turned on in response to the second sampling clock.

25. (Currently Amended) The image processing system of claim [[24]]15, wherein the overall gain is pseudo-logarithmic.

26. – 39. (Cancelled)

40. (Currently Amended) A method of processing an image, comprising:

providing a correlated double sampler (CDS) for receiving an input signal, sampling the input signal, amplifying the input signal with a first gain of the CDS, [[and]] providing an output signal, ~~and amplifying the input signal, the CDS comprising a variable capacitance unit having first and second variable input capacitances for setting gain in the CDS, the first variable input capacitance being connected to a first input of an amplifier and the second variable input capacitance being connected to a second input of the amplifier~~ and setting the first gain to one of a plurality of first levels based on a digital input signal; [[and]]

providing a programmable gain amplifier (PGA) for receiving the output signal from the CDS and amplifying the received output signal with a second gain of the PGA; and

setting the second gain to one of a plurality of second levels based on the digital input signal, each of the first levels being divided into the second levels, and an overall gain being determined by a combination of the first gain of the CDS and the second gain of the PGA.

41. (Cancelled)

42. (Cancelled)

43. (Currently Amended) The method of claim 40, ~~further comprising setting gain in the CDS~~ wherein setting the first gain comprises setting the first gain to a level between 1.0 and 2.0.

44. (Cancelled)

45. (Currently Amended) The method of claim 40, wherein ~~further comprising~~ setting the second gain ~~in the PGA~~ comprises setting the second gain to a level between 1.0 and 2.0.

46. (Cancelled)

47. (Currently Amended) The method of claim [[46]]40, wherein the digital input signal contains a plurality of bits.

48. (Currently Amended) The method of claim 47, wherein ~~a first portion of the bits is applied to the CDS to set gain in the CDS and a second portion of the bits is applied to the PGA to set gain in the PGA~~the first gain of the CDS is settable to one of the first levels based on a first portion of the bits and a second gain of the PGA is settable to one of the second levels based on a second portion of the bits.

49. (Cancelled)

50. (Currently Amended) The method of claim [[49]]40, wherein the overall gain is pseudo-logarithmic.

51. (New) The image processing system of claim 24, wherein active periods of the second sampling clock do not overlap with active periods of the first sampling clock.

52. (New) The image processing system of claim 24, wherein the first reference level signal has a first level, the second reference level has a second level, and the third reference level has a third level, the first level being lower than the second level, and the second level being lower than the third level.

53. (New) The image processing system of claim 15, wherein the PGA comprises:

a second amplifier having an inverted input terminal, a non-inverted input terminal, an inverted output terminal, and a non-inverted output terminal;

a first switch array having a first plurality of switches, each of the first switches having a first terminal, a second terminal, and a third terminal, the first terminal coupled to a non-inverting output terminal of the first operational amplifier, the second terminal coupled to the non-inverting output terminal of the second operational amplifier, the third terminal receiving one of the first, second, and third reference level signals, each of the first switches switching the first, second, and third terminals to a first common terminal in response to the second sampling clock and a second portion of a plurality of bits of the digital input signal;

a first plurality of capacitors respectfully coupled to the inverted input terminal of the second operational amplifier and first common terminals of the first switch array;

a second switch array having a second plurality of switches, each of the second switches having a fourth terminal, a fifth terminal, and a sixth terminal, the fourth terminal coupled to an inverting output signal of the first operational amplifier, the fifth terminal coupled to the non-inverting output terminal of the second operational amplifier, the sixth terminal receiving one of the first, second, and third reference level signals, each of the second switches switching the fourth, fifth, and sixth terminals to a second

common terminal in response to the second sampling clock and the second portion of the plurality of bits of the digital input signal; and

a second plurality of capacitors respectively coupled to the non-inverted input terminal of the second operational amplifier and second common terminals of the second switch array.

54. (New) The image processing system of claim 53, wherein the first and second sampling clocks are generated from an overlap prevention circuit, and the overlap prevention circuit includes:

a first input buffer for buffering a first clock;

a second input buffer for buffering a second clock to output a fourth clock;

a first logic circuit for performing a first logic operation on an output signal of the first input buffer and a first feedback signal;

a second logic circuit for performing a second logic operation on an output signal of the second input buffer and a second feedback signal;

a first delay circuit for delaying an output signal of the first logic circuit to generate the second feedback signal;

a second delay circuit for delaying an output signal of the second logic circuit to generate the first feedback signal;

a first output buffer for buffering the second feedback signal to generate the first sampling clock; and

a second output buffer for buffering the first feedback signal to generating the second sampling clock.

55. (New) The image processing system of claim 53, wherein the first sampling clock has an inverted phase with respect to the second feedback signal, and the second sampling clock has an inverted phase with respect to the first feedback signal.